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Express Mail Label No.: EV154826857 US *Attorney Docket No.: D5116-00002*

PATENT

In re application of: Saxena et al.

Examiner: Russell Warren Frejd

Serial No.: 09/675,427

Group Art Unit: 2123

Filed: September 29, 2000

Petition to Make Special Under 37 CFR 1.102(d) and MPEP 708.02 (VIII)

For: EFFICIENT METHOD FOR MODELING AND SIMULATION OF THE IMPACT OF LOCAL AND GLOBAL VARIATION ON INTEGRATED CIRCUITS

I, PATRICIA A. MCINTOSH, HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231

on October 18 2002 *EXPRESS MAIL LABEL NO.* ***EV154826857US***

Patricia A. McIntosh

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PETITION TO MAKE SPECIAL UNDER 37 C.F.R. 1.102(d) AND M.P.E.P. 708.02(VIII)

Applicants hereby petition under 37 C.F.R. 1.102(d) and M.P.E.P. 708.02 (VIII) that the subject application be granted special status and advanced in order of examination. Applicants submit that all of the claims are directed to a single invention. Accompanying this petition are:

(1) a statement that a pre-examination search was made by a foreign patent office and a detailed discussion of the references identifying how the claimed subject matter is patentable over the references;

(2) a copy of each of the references deemed most closely related to the subject matter encompassed by the claims; and

(3) the petition fee set forth in 37 C.F.R. § 1.17(i).

Respectfully submitted,

Dated: 10/18/02

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PATENT

In re application of: Saxena et al. Examiner: Russell Warren Frejd

Serial No.: 09/675,427 Group Art Unit: 2123

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ON October 18 2002 *EXPRESS MAIL LABEL NO.* ***EV154826857US***

Patricia A. McIntosh

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

STATEMENT AND DISCUSSION ACCOMPANYING PETITION TO MAKE SPECIAL UNDER 37 C.F.R. 1.102(d) AND M.P.E.P. 708.02(VIII)

Applicants hereby state that, according to the information provided by the International Preliminary Examining Authority, a preliminary examination search was conducted by the International Preliminary Examining Authority in the following fields:

(1) IPC(7): G06F 7/60, 17/50

(2) US Cl.: 703/2, 14; 716/1, 8

The six (6) references deemed most closely related to the subject matter encompassed by the claims and cited by the International Preliminary Examining Authority, which are already of record, are listed as items 1-6 below. Also listed below are forty-five (45) additional references already of record in this application.

Following is a detailed discussion of the enclosed references, pointing out the differences between each of the cited references and the Applicants' claimed invention. None of the following references discloses or suggests reducing the complexity of statistical simulation by performing a first level principal component or principal factor decomposition of global variation, including screening. Furthermore, none of the following references discloses or suggests reducing the complexity of statistical simulation by performing principal component or principal factor decomposition for local mismatch, including screening.

(1) US 6,066,179 to Allan - discloses a method and apparatus to estimate properties of an integrated circuit device utilizing reduced resources, wherein a property of an integrated circuit is determined from an analysis of a fraction of the integrated circuit representation.

(2) "Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect" by Conti, M. et al. - discloses a model for predicting a dependence of correlation, between devices fabricated in the same die, on their dimensions and mutual distances to that mismatch between equally designed devices can be considered as a particular case of such a model.

(3) "Mismatching Modeling and characterization of Bipolar Transistors for Statistical CAD" by To, H. et al. - discloses a test structure and method for studying the parameter mismatch variance for vertical npn bipolar transistors. The objective is to determine if the collector current mismatch of a BJT pair at any bias can be represented by two BJT parameter mismatches; I_n and λ.

(4) "Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's" by Felt, E. et al. - discloses a methodology for measuring MOS transistor current mismatch based on extracting the mismatch information from a fully functional circuit rather than on probing individual device, wherein the model characterizes the total mismatch as a sum of two components, one systematic and the other random.

(5) "A Flexible Statistical Model for CAD of Submicrometer Analog CMOS Integrated Circuits" by Michael, C. et al. - discloses a statistical model for computer-aided design of submicrometer analog integrated circuits, wherein the model accounts for both parameter mismatch and inter-die parameter variations.

(6) "Incorporating MOS Transistor Mismatches Into Training of Analog Neural Networks" by Ogrenci, A. et al. - discloses a model for training an analog neural

network, wherein mismatch characteristics in the threshold voltages and current factors of the synapse, opamp, and sigmoid circuitry of the analog neural network are analyzed.

(7) US 3,751,647 to Maeder et al. - discloses yield modeling for an integrated circuit manufacturing process utilizing the number of defects for each chip, rather than average defect density, in the prediction model.

(8) US 4,795,964 to Mahant-Shetti et al. - discloses a combination inverter chain and ring oscillator for measuring the capacitance of a field effect transistor device by measuring the current associated with propagating a signal through the circuit at a certain signal frequency.

(9) US 4,835,466 to Maly et al. - discloses detecting spot defects in integrated circuits utilizing an apparatus which comprises a meander structure formed in a high resistivity material on a substrate. Defects are identified by measuring the resistance between the ends of the meander. If the measured value of resistance is substantially smaller than the calculated value, a flaw due to a spot of additional high conductivity material is considered to be present. If the measured resistance is substantially greater than the calculated resistance, a flaw due to a spot of missing high conductivity material is determined to exist.

(10) US 4,939,681 to Yokomizo et al. - discloses a circuit simulation method and apparatus for simulating the operation of semiconductor devices on the basis of the mask layout pattern of each semiconductor device. An equivalent circuit of the semiconductor device is determined from the mask layout patterns, and then a signal indicative of the operation of the equivalent circuit is produced.

(11) US 5,067,101 to Kunikiyo et al. - discloses a topography simulation method for estimating the three-dimensional shape of a surface of a workpiece where material removal by a predetermined process takes place. The simulation method includes the steps of dividing a region of the workpiece to be removed into a plurality of partial regions; setting a diffusion coefficient for each partial region with a diffusion component contributing to materiel removal, and calculating a contour surface of the concentration of the diffusion component by a process which employs modified diffusion equations.

(12) US 5,068,547 to Gascoyne - discloses a process monitoring method and circuit for monitoring process steps for manufacturing P and N transistors. The process monitor circuit provides first and second logic paths, the first logic path has a delay sensitive to whether the input logic transition is from logic high to logic low, or from logic low to logic high. The second logic path has substantially equal delays for either logic state transition. The two differences in

delay between the first and second logic paths under the two logic state transitions are used to monitor the process steps.

(13) US 5,070,469 to Kunikyo et al. - discloses a topography simulation method for simulating a surface topography of a materiel object material while a surface of material object is being processed, as by etching or a deposition. The method includes the steps of dividing a region to be analyzed, in a surface including the advancing direction of processing, into a plurality of regions in a grid in accordance with the surface topography of the material object by approximating the movement of the processed surface of the material object as the movement of an equi-concentration surface determined by the diffusion of particles, establishing diffusion coefficients for the respective regions on the basis of the surface processing velocity, calculating equi-concentration surfaces by the Diffusion equation, and assembling the obtained equi-concentration surfaces to produce a three-dimensional surface topography.

(14) US 5,286,656 to Keown et al. - discloses a method of fabricating and testing integrated circuits(IC) on a wafer and a new wafer structure for individualized prepackage testing of the IC dies on the wafer before scribing and packaging. Individualized prepackage testing of AC performance of a selected sensitive AC parameter for all dies on the wafer at the wafer level stage during DC parametric testing is provided.

(15) US 5,301,118 to Heck et al. - discloses a two-stage Monte Carlo method of tolerancing components of an assembly. The mean and the standard deviation of the individual component features are mathematically shifted or adjusted in a Monte Carlo simulation to account for changes in feature dimensions over time. These shifted or adjusted parameters are utilized in a subsequent Monte Carlo simulation to determine discrete values for the individual points of each output distribution. The individual points of the output distributions are then combined for individual assembly final fit.

(16) US 5,438,527 to Feldbaumer et al. - discloses a method for predicting yields for integrated circuit designs for given specification limits and process variations with respect to transistor parametric variations based on a statistical analysis starting with response surface modeling techniques that relate desired circuit outcomes as a function of a set of defined independent variables. The response surfaces are converted to discrete C_{pk} surfaces for all combinations of the independent variables. The C_{pk} surfaces for each of the circuit outcomes winch then are combined to provide a composite yield surface comprising all desired parametric operating points of the outcomes that may be used to predict the circuit yield.

(17) US 5,486,786 to Lee - discloses a process monitor for a CMOS integrated circuit including first and second delay units that are connected in a ring to constitute a ring oscillator that generates pulses having different phases at the outputs of the delay units respectively The delay units affect the frequency of the pulses and also the rising and falling edges of the pulses differently depending on the process factor of PMOS and NMOS transistors in the delay units.

(18) US 5,502,643 to Fujinaga - discloses a method and apparatus for setting up parameters which are used to manufacture a semiconductor device. Using parameters which are necessary for attaining a threshold voltage of a semiconductor device, process simulation is performed to thereby compute the threshold voltage. Whether the computed threshold voltage has a predetermined value is then judged. The parameters are updated until he predetermined value is reached.

(19) US 5,625,268 to Miyanari - discloses a stepping motor drive circuit including a bridge circuit composes of energizing coils constituting a stepping motor and four transistors, and current value switching circuitry for selecting a value of current flow according to the rotation direction of the stepping motor.

(20) US 5,627,083 to Tounai - discloses a method of fabricating a semiconductor device including the steps of forming a inner circuit, a cell test pattern, and a superposition error measurement pattern. The inner circuit includes a plurality of recurring basic cells. The cell test pattern includes a test cell array having at least one test basic cell of the same design as the basic cells in the inner circuit and a plurality of test dummy cells disposed around the test cell array. The superposition error measurement pattern includes a first and a second pattern formed in the steps of a first and a second lithographic step, respectively, performed in the formation of the basic cells.

(21) US 5,629,877 to Tamegaya - discloses a unified process and device simulation system for performing simulation for a process design and a device design of a semiconductor device. The system includes a process simulator, which performs a process simulation for one of a pair of regions of the semiconductor device symmetric in configuration and structure about a center line which extends perpendicular to a direction about which the simulation is carried out. The process simulator generates a first simulation data. The system also includes a mirror reversal processing portion for performing a mirror reversing process for establishing a mirror data of the first simulation data symmetric about the center line on the basis of structure data of the semiconductor and connecting the mirror data to the first simulation data at the center line in order to generate a second data equivalent to a process simulation data obtained through the process

simulation for an entire region of the semiconductor device. A device simulator then performs a device simulation with respect to the second data on the basis of a predetermined analysis condition.

(22) US 5,655,110 to Krivokapic et al. - discloses a method for setting and adjusting process parameters to maintain acceptable critical dimensions across each die of mass produced semiconductor wafers. The method includes the steps of matching a machine implemented process simulator with an actual fabrication line, using the matched model to simulate the statistical results of mass production by the modeled production line, using the model to predict cross-reticle variance from collected data for in scribe features, using the model to decompose the variance contributions of each process parameter and identify the more prominent contributors, and using the model to identify the process parameter adjustments which would provide best leverage when taken one at a time.

(23) US 5,703,381 to Iwasa et al. - discloses a semiconductor integrated circuit including a rectangular semiconductor chip having a main surface, a plurality of pads formed in a peripheral portion of the main surface of the semiconductor chip, for connection to external connecting members, a plurality of circuit elements of an integrated circuit formed in an area of the main surface other than an area in which the plurality of pads are formed, and at least one characteristic evaluating circuit element connected to at least one of the plurality of circuit elements of the integrated circuit by sharing a impurity doped region which forms part of the at least one circuit element with the at least one circuit element of the integrated circuit in an aria of the main surface other than he peripheral portion in which the plurality of pads are formed.

(24) US 5,767,542 to Nakamura - discloses a CMOS layout for enabling the creation of matching parasitic capacitance and characteristics of field effect transistors to an existing parasitic capacitance and characteristics of field effect transistors. Cross coupling of matched capacitance and other characteristics are used to cancel effects resulting from the capacitance and other characteristics.

(25) US 5,773,315 to Jarvis - discloses a method for predicting yield value for a silicon wafer subjected to a wafer fabrication process. The wafer fabrication process forms multiple integrated circuits upon a surface of the wafer. A unit cell region is chosen on the surface of the wafer. Two or more masking steps, which form features within the selected unit cell region are chosen as critical masking steps. Portions of the unit cell region are identified as critical regions. A fraction of the unit cell region enveloped by critical regions is used to compute a critical chip area A' for the critical masking step. An electrical fault density D' is computed for each critical masking step as a product of an expected total defect

density D, and a fraction of defects expected to result in catastrophic failures. An estimated yield value is calculated for each critical making step by substituting A" and D' for A and D, respectively, in a yield equation associated with an existing yield prediction model.

(26) US 5,778,202 to Kuroishi et al. - discloses a ring bus multiprocessor system having processors are laid out and serially connected by communication buses to form a processor group. Each processor board may have an even number plurality of processor groups mounted thereon. A plurality of processor boards are laid out in parallel and are interconnected between adjacent boards by means of inter processor communication buses. Each of the odd number processor groups is connected from one board tot he next up to the most downstream board where the connection is looped back to the adjacent even numbered processor group. In turn the even numbered processor group is connected from one board to the next back to the most upstream bard where the connection is again looped back to the adjacent odd numbered processor group, and so on, whereby a ring bus arrangement is formed.

(27) US 5,790,479 to Conn - discloses using a ring oscillator circuit to determine timing characteristics of a test interconnect structure in an integrated circuit. Reference timing characteristics of the unloaded reference ring oscillator circuit are determined according to a calibration method including the steps of directly measuring signal propagation delay through each segment of the oscillator circuit, modeling each test segment using an RC tree type reference circuit model having reference elements, simulating the reference circuit model to provide a functional relationship between two reference capacitors, defining upper and lower bounds for propagation delay through the test segment in terms of the reference elements, determining values for the reference capacitor elements, and measuring a reference frequency of oscillation of the unloaded oscillator circuit.

(28) US 5,798,649 to Smayling et al. - discloses a method for determining the reliability of thin film insulators with noise measurement which find the barrier height mean and standard deviation. A constant voltage source is applied across the thin film insulator. A low noise amplifier is connected across a resistor, which is in series with the insulator. A spectrum analyzer is connected to the low noise amplifier. The power density is obtained by observing the output of a spectrum analyzer. The current spectral density is compared to a predetermined reference to detect the presence of defects in the insulator.

(29) US 5,822,258 to Casper - discloses a method for testing a memory device by writing test data to an array of cells of the memory device during a test mode and driving a cell plate of the memory device during at least a portion of the test with

a current level that is less than the current used during normal operation. This results in the affect on the cell plate voltage of defective cells being amplified and allowing identification of same.

(30) US 5,852,581 to Beffa et al. - discloses a method and apparatus for stress testing a memory integrated circuit die. A burn-in power supply voltage and a ground voltage are supplied to each memory die of a plurality of memory die on a semiconductor wafer. This burn-in power supply voltage is provided to a cell plate common node of a memory cell storage capacitor. A ground voltage is provided to at least one bit line of a plurality of bit lines. At least one cell access transistor is turned on, thereby allowing conduction between the bit line and a storage node of the memory cell storage capacitor. A ground voltage is also provided to the common cell plate of the storage capacitor and the burn-in power supply voltage is provided to at least one bit line of the plurality of bit lines, thus creating stress conditions of differing polarities capable of being coupled across the memory cell storage capacitor dielectric and the cell access transistor.

(31) US 5,867,033 to Sporck et al. - discloses a circuit for testing a semiconductor device having an oscillator for producing pulses when energized. The oscillator pulses have a frequency, which corresponds to operational characteristics of the semiconductor device. A control circuit receives a test signal, a clock signal having pulses, and a reset signal, and energizes the oscillator for a predetermined length of time in response to the test signal. A counter detects the pulses produced by the oscillator, and produces counter signals, which indicate the number of pulses detected by the counter. An output circuit produces an output corresponding to the count, which indicates at least one of the operational characteristics of the semiconductor device.

(32) US 5,903,012 to Boerstler - discloses a process variation monitor for sensing transistor parameters and supplying a compensation signal. The process variation monitor, monitors fabrication variations by utilizing a first and second transistor. The first transistor can be an un-implanted or a partially implanted transistor. The second transistor can be a conventional, fully implanted transistor or a partially implanted transistor. The second transistor has parameters, which reflect process variations. The transistors are biased to create a signal in the first transistor that varies proportionally to the parameters of the second transistor, thus allowing process induced parameters of the second transistor to be monitored by the first transistor.

(33) US 5,966,527 to Krivokapic et al. - discloses simulating mass produced semiconductor behavior by obtaining drain to source current values from actual semiconductor devices in response to voltage levels at the drain to source and gate

of a semiconductor device. Semiconductor device attributes are also measured. A device simulator and process simulator are calibrated based upon the actual drain to source current values and measured attributes. The process simulator is run in response to simulated process parameters to obtain a plurality of simulated mass produced semiconductor devices having varying semiconductor attributes. The device simulator is then run using the plurality of simulated mass produced devices to obtain a plurality of I/V curves based upon the plurality of simulated semiconductor device.

(34) US 5,982,929 to Ilan et al. - discloses a pattern recognition method for pattern recognition of indicia composed of alphabetical characters of a language in the form of at least a part of a word. A probability value designating the relative confidence in the recognition of the character as one of the language characters is assigned to each character. The established shapes of the characters are then sequentially applied to a linguistic recognizer for further processing and the probability values of language structure to each of the language characters is assigned. Then the probability values assigned to the characters in the shape recognizer are combined with the corresponding probability values assigned to the characters in the linguistic recognizer and the path between characters possessing the highest probability values is determined.

(35) US 6,005,829 to Conn - discloses a reference ring oscillator used to determine timing characters of a test interconnect structure in an integrated circuit. The oscillator circuit includes an odd number of inverters coupled together in a ring manner and has defined test segments at which a test interconnect can be loaded. Reference timing characteristics of the unloaded reference ring oscillator circuit are determined according to a calibration method including the steps of directly measuring signal propagation delay through each segment of the oscillator circuit, modeling each test segment using an RC tree type reference circuit model having reference elements, simulating the reference circuit model to provide a functional relationship between two reference capacitors, defining upper and lower bounds for propagation delay through the test segment in terms of the reference elements, determining values for the reference capacitor elements, and measuring a reference frequency of oscillation of the unloaded oscillator circuit. Timing characteristics of the test interconnect are determined in based on measured time differences and determined reference timing characteristic of the test segment.

(36) US 6,063,132 to DeCamp et al. - discloses a method for using a generate and verify computer program product to generate, by repetitive passes, a design rules checking computer program for generating and verifying a design rules description file for use with a general purpose shapes processing program.

Design rule checking is the process for ensuring that VLSI masks are created according to the proper layout criteria. The design rules are described in a file called a runset. The runset is repeatedly executed in loop fashion with respect to a test case file containing groups of layout structures or shapes used for verifying the correctness of the runset.

(37) US 6,072,804 to Beyers, Jr. - discloses a ring bus data transfer system including a plurality of nodes coupled together by a ring bus for transmitting data in successive bus cycles, each bus cycle containing a plurality of bus words. One of the bus words in the bus cycle is a bus cycle synchronization word and the remainder of which are data words. The plurality of data words are allocated to a plurality of data channels.

(38) US 6,075,417 to Cheek et al. - discloses a ring oscillator test structure including an odd plurality of first transistor pairs formed on a predetermined area of a semiconductor substrate. The transistor pairs are electrically connected in a serial ring. The structure also includes at least one second transistor pair, also formed within the predetermined area on the substrate, but electrically isolated form the odd plurality of first transistor pairs.

(39) US 6,075,418 to Kingsley et al. - discloses a circuit for separately measuring a selected one of the rising edge and falling edge signal propagation delays through one or more circuits of interest. A number of synchronous components are configured in a loop so that they together from a free running ring oscillator. The oscillator produces an oscillating test signal in which the period is proportional to the clock-to-out delays of synchronous components.

(40) US 6,118,137 to Fulford, Jr. et al. - discloses a method for determining lithographic misalignment of a conductive element relative to a via. An electrically measured test structure is provided which is designed to have targeted via areas shifted form midlines of corresponding targeted conductor areas. Design specifications of the test structure require the midlines of the conductor areas to be offset from the via areas by varying distances. The test structure is processed and an electrical signal is then applied to each of the conductors while it is also being applied to a test pad. The resulting electrical response is proportional to the distance that a conductor is misaligned from its desired location.

(41) US 6,124,143 to Sugasawara - discloses process monitoring circuitry incorporating additional routing structures that approximate signal delays due to long metal routing paths. Supplemental metal routing lines are disposed in unused routable silicon space, such that no silicon area penalty is suffered as a

result of having long metal routing lines. During testing of an integrated circuit, test signals are compared to simulated delay values that reflect the delays of the additional metal routing lines and vias.

(42) US 6,134,191 to Alfke - discloses a circuit for separately measuring one or both of the rising edge and falling edge signal propagation delays through a signal path of interest. To determine the delay through the signal path, the signal path is used with a second, typically identical, signal path to create alternating feedback paths of an oscillator. The oscillator is configured to output a test clock signal having a period proportional to either the rising or falling edge delays through the two signal paths. The average period of the oscillator is related to the average signal propagation delay through the signal path of interest.

(43) US 6,184,048 to Ramon - discloses a method for assuring quality and reliability of semiconductor integrated circuit devices, fabricated by a series of documented process steps, comprising: (1) electrically testing the devices outside their specified operating voltage range, yet within the capabilities of the structures produced by the process steps, thereby generating raw electrical test data; (2) comparing the test data to values expected from the design of the devices, thereby providing nonelectrical characterization of the devices to verify compositional and structural features; and (3) correlating the features with the documented process steps to find deviations therefrom, as well as structural defects, thereby identifying outlier devices.

(44) "A Novel Approach for Reducing the Area Occupied by Contact Pads on Process Control Chips" by Walton et al. - discloses an approach for reducing the number of pads required by electrical test structures utilizing a multiplexing scheme requiring only two levels of interconnect. The number of electrical connections are divided into groups, each group having one terminal of each component connected to a single pad. The other end of each component is connected to the access terminals in such a manner that no two components in the same group are connected to the same pad.

(45) "The Spidermask: A New Approach for Yield Monitoring Using Product Adaptable Test Structures" by Beckers and Hilltrop - discloses a method of yield monitoring based on the use of a product specific test structure. The test structure, referred to as a spidermask, isolates and contacts individual structures to create a complete yield monitor set. Instead of processing a complete test vehicle, as in done in the case of a traditional yield monitor, this approach starts with the existing design of a high volume running product. This product is then processed up to the contact level. At that point, a specially designed spidermask, in

combination with the appropriate contact mask, is used to create, on the product underground, the required yield monitor test structure.

(46) "Understanding Across Chip Line Width Variation: The First Step Toward Optical Proximity Correction" by Liebman et al. - discloses that a prerequisite to successful optical proximity correction is an in depth understanding of the relevant parameters leading to patterning inaccuracies. This papers investigates sources of 1-dimensional line width errors, deemed the most critical for optical proximity correction. It is asserted that pattern density has a very significant effect on line width and that lithography, not just reactive ion etch, is significantly impacted by pattern density.

(47) "Extraction of Defect Characteristics for Yield Estimation Using The Double Bridge Test Structure" by Khare et al. - discloses using a Double Bridge Test Structure to extract defect characteristics for accurate yield estimation. Specifically, the Double Bridge Test Structure is used to obtain defect size distribution in the metal layer.

(48) "Evaluating the Manufacturability of GaAs/AlGaAs Multiple Quantum Well Avalanche Photodiodes Using Neural Networks" by Yun et al. - discloses a approach for parametric yield prediction of GaAs/AlGaAs multiple quantum well (MQW) avalanche photodiodes (APDs). Using a small number of test devices with varying active diameters, barrier and well widths, and doping concentrations relatively accurate prediction of the expected performance variation of APD gain and noise in larger populations of devices are enabled. Neural networks are used to generate the models to characterize the manufacturing variations.

(49) "Effectiveness of Yield-Estimation and Reliability-Prediction Based on Wafer Test-Chip Measurements" by Hansen et al. - discloses the use of dropped in test chips as an instrument for monitoring the quality of each manufacturing step of VLSI chips, and as a mechanism for eliminating potentially bad wafers. The yield and long term reliability are estimated on the basis of the test chips manufactured on the same wafer as the fully functional chips. A Monte Carlo simulation model is provided that allow comparison of yield estimates with actual wafer yields, under various scenarios of defect density variation, test structure scaling factor, and test chip sample size and location within the wafer.

(50) "In-Line Yield Prediction Methodologies Using Patterned Wafer Inspection Information" by Nurani et al. - discloses a multilayer critical area method and a defect type size kill ratio method for in-line prediction of yield. The multilayer critical area method utilizes the design layout information along with the in-line

defect data, whereas the defect type size kill ratio method utilizes the defect and yield data to empirically derive the kill ratios.

(51) "Yield Oriented Computer-Aided Defect Diagnosis" by Khare et al. - discloses an investigation of an inductive fault analysis based defect methodology to see if it provides the ability to perform rapid defect diagnosis for yield learning and if it provides the ability to efficiently extract defect parameters from the manufacturing line.

Applicants have particularly and distinctly claimed an invention, which is distinguishable from the prior art cited herein. In addition, Applicants have complied with all the necessary requirements for affording the above-identified application special status. Accordingly, Applicants request that the application be made Special pursuant to 37 CFR §1.102(d) and advance in the order of examination.

Respectfully submitted,

Dated: 10/18/02

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